IN THE CLAIMS:

Please cancel Claims 2-6 without prejudice or disclaimer.

Claim 1 (original): A drive circuit to supply drive current to a load resistor that is connected to a first power voltage supply element, comprising:

a current output MOS transistor connected in series with the load resistor,

a drive part that is connected to a second power voltage supply element and that supplies a drive signal to the gate terminal of the current output MOS transistor, and

a clamp circuit that is connected to the second power voltage supply terminal to hold the drain terminal of the current output MOS transistor at a predetermined potential.

Claims 2 – 6 (cancelled)

Claim 7 (original): The drive circuit of Claim 1, wherein the drive part includes:

a fourth MOS transistor that is connected to the gate terminal of the current output MOS transistor and that supplies a drive signal to the current supply MOS transistor, and

a second current source that supplies current to the fourth MOS transistor.

Claim 8 (original): The drive circuit of Claim 7 wherein the drive part comprises a third current source that is connected between the source terminal and the reference potential of the fourth MOS transistor, which is an NMOS transistor, and a fifth NMOS transistor that is connected between the second current source and the reference potential and that operates complementarily with the fourth NMOS transistor, and

the second current source comprises a third PMOS transistor that is connected between the second power supply voltage terminal and the fifth NMOS transistor and whose gate terminal and drain terminal are connected, and a fourth PMOS transistor that is connected between the second power supply voltage terminal and the middle connection point between the gate terminal of the current output MOS transistor and

the fourth NMOS transistor, and whose gate terminal is connected to the gate terminal of the third PMOS transistor.

Claim 9 (original): The drive circuit of Claim 8 wherein the drive part has a second resistive element that is connected between the drain terminal of the third PMOS transistor and the drain terminal of the fifth NMOS transistor, and a third resistance terminal that is connected between the second power supply voltage terminal and the gate terminal of the third PMOS transistor.